REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application and indicating that claims 8, 19, and 30 contain allowable subject matter.

I. Disposition of Claims

Claims 1-33 are currently pending in the present application. By way of this reply, claims 1, 12, and 23 have been amended.

II. Claim Amendments

Claim 1 has been amended to clarify that the method of claim 1 comprises simulating operation of the phase locked loop using the digitized representatively power supply waveform having noise as a power supply input to the phase locked loop. Further, claim 1 has been amended to remove the limitation "inputting the digitized representative power supply waveform having noise into a simulation of the phase locked loop." No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figures 5a and 7 of the present application.

Claims 12 and 23 have been amended to clarify that the referred-to instructions are used to simulate operation of the phase locked loop using the digitized representatively power supply waveform having noise as a power supply input to the phase locked loop. Further, claims 12 and 23 have been amended to remove the limitation that the referred-to instructions are used to "input the digitized representative

power supply waveform having noise into a simulation of the phase locked loop." No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figures 5a and 7 of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1-7, 9-18, 20-29, and 31-33 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by Jenkins et al. ("Measuring Jitter and Phase Error in Microprocessor Phase-Locked Loops," Keith A. Jenkins and James P. Eckhardt, IEEE Design and Test of Computers, April – June 2000, pages 86-93). For the reasons set forth below, this rejection is respectively traversed.

The present invention is directed to a technique for estimating/determining jitter of a phase locked loop based on a simulation of the phase locked loop. *See* Specification, paragraph [0025]. With reference to the exemplary flow process shown in Figure 5a of the present application, a technique in accordance with the present invention involves (i) obtaining a representative power supply waveform having noise **172**, (ii) digitizing the representative power supply waveform having noise **174**, and (iii) simulating operation of a phase locked loop using the digitized representative power supply waveform having noise as a power supply input to the phase locked loop **176** (*see also* Specification, paragraph [0028]). Using a digitized representative power supply waveform as a power supply input to the phase locked loop leads to more accurate simulation than with those simulation techniques that use analog power supply waveforms (*e.g.*, square waves as shown in Figure 4 of the present application). *See* Specification, paragraph [0028]. Further, the use of a digital power supply leads to more efficient and faster simulation

due to a reduced amount of overhead with respect to data points needing to be processed. *See* Specification, paragraph [0028]. Accordingly, amended independent claims 1, 12, and 23 of the present application require that the digitized representative power supply waveform having noise serve as an input to the phase locked loop being simulated.

Jenkins et al., in contrast to the present invention, fails to disclose all the limitations recited in amended independent claims 1, 12, and 23 of the present application. Jenkins et al. clearly discloses an analog, not a digital, signal that serves as a *power supply input* to the phase locked loop. For example, as shown in Figure 6 of Jenkins et al., a noise generator circuit "introduces noise on the PLL power supply" (*see* Jenkins et al., page 89, lines 21 – 27) using an "external resistor (R_{ext}) [that] causes a change in the *analog* supply-voltage level." Jenkins et al., page 89, lines 27 – 31 (emphasis added). This analog PLL power supply, $\mathbf{V_{DDA}}$, serves as the power supply input to the phase locked loop. There is no digitization of the supply voltage $\mathbf{V_{DDA}}$ before it is input to the PLL. Further, Jenkins et al. repeatedly and specifically refers to the power supply voltage $\mathbf{V_{DDA}}$, which serves as the power supply input to the PLL (Figure 6 of Jenkins et al.), as an "analog voltage." *See, e.g.*, Jenkins et al., page 91, line 33; Jenkins et al., page 91, lines 40; Figure 7 of Jenkins et al.

Thus, regardless of whether the supply voltage $\mathbf{V_{DDA}}$, as exemplarily shown in Figure 6 of Jenkins et al. is later digitized by an oscilloscope, or other measurement device, Jenkins et al. does not disclose applying a *digitized* power supply waveform *as a power supply input* to the phase locked loop as required by amended independent claims 1, 12, and 23 of the present application. Instead, as discussed above, the supply voltage $\mathbf{V_{DDA}}$ to the phase locked loop in Jenkins et al. is clearly an analog signal, and is

purposefully intended to be an analog signal as is apparent from the teachings & disclosure found in Jenkins et al.

In view of the above, Jenkins fails to show or suggest the present invention as recited in amended independent claims 1, 12, and 23 of the present application. Thus, amended independent claims 1, 12, and 23 of the present application are patentable over Jenkins. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.170001;P7188).

Respectfully submitted,

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Jonathan P. Osha, Reg. No. 33,986
ROSENTHAL & OSHA L.L.P.
1221 McKinney Street, Suite 2800
Houston, TX 77010

Telephone: (713) 228-8600
Facsimile: (713) 228-8778

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